Qualification Results Summary AD5755-1 LFCSP

QUALIFICATION PLAN / STATUS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
High Temperature Operating Life (HTOL)*	JEDEC *JESD22-A108*	**9 x 45**	**Pass**
Highly Accelerated Stress Test (HAST)*	JEDEC *JESD22-A110*	**9 x 45**	**Pass**
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	**9 x 45**	**Pass**
Temperature/Humidity/Bias (THB)*	JEDEC *JESD22-A101*	**3 x 77**	**Pass**
High Temperature Storage Life (HTSL)	JEDEC *JESD22-A103*	**3 x 77**	**Pass**
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	**9 x 11**	**Pass**
Latch-Up	JEDEC *JESD78*	**±100mA**	**Pass**
Electrostatic Discharge *Human Body Model*	ESDA/JEDEC *JS-001*	**3/voltage**	**Pass ±1.8kV**
Electrostatic Discharge *Machine Model*	JESD22-A115	**3/voltage**	**Pass ±100V**
Electrostatic Discharge *Field-Induced Charged Device Model*	JEDEC *JESD22-C101*	**3/voltage**	**Pass ±1.0kV**

*Preconditioned per JEDEC/IPC J-STD-020

TIMING CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; AV_{SS} = −15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	50	ns min	SCLK cycle time
t_2	17	ns min	SCLK high time
t_3	17	ns min	SCLK low time
t_4	20	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	15	ns min	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge (see Figure 79)
t_6	**500**	**ns min**	**$\overline{SYNC}$ high time following a configuration write**
	5	µs min	SYNC high time following a DAC update write
	20	**µs min**	**SYNC high time following a DAC update write (slew rate control enabled)**
t_7	15	ns min	Data setup time
t_8	10	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel with digital slew rate control enabled; single DAC updated)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel with digital slew rate control disabled; single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	**520**	**ns max**	**$\overline{LDAC}$ falling edge to DAC output response time**
t_{12}	See the AC Performance Characteristics section	µs max	DAC output settling time
t_{13}	**5**	**µs min**	**CLEAR high time**
t_{14}	**9**	**µs max**	**CLEAR activation time**
t_{15}	**45**	**ns max**	**SCLK rising edge to SDO valid**
t_{16}	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	1	µs min	$\overline{RESET}$ pulse width

[1] Guaranteed by design and characterization; not production tested.
[1] All input signals are specified with t_R = t_F = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[1] See Figure 3, Figure 4, Figure 6, and Figure 7.

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 6, and Figure 7.